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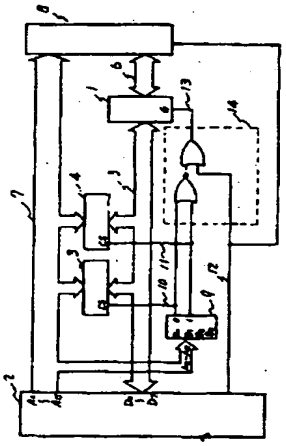
Applicant: NEC CORP
Inventor: ISHIDA AKIRA
CPU PERIPHERAL CIRCUIT

Abstract:

PURPOSE: To protect the memory operation from noise of peripheral elements and at the same time to improve the capacity of a bus buffer, by providing a bus buffer control circuit to control the separation/connection between two data buses with a control signal.

CONSTITUTION: A CPU2 is connected to memories 3 and 4 with a data bus 5, and a peripheral element 8 is connected to a bus buffer 1 via a data bus 6 and separated from the bus 5 by the buffer 1. Memory selection signals 10 and 11 are supplied at logic level "1" when the memories are selected. The buffer 1 is active when the logic level "1" is supplied to a control input G. In case the actuation is carried out between a memory 3 or 4 and the CPU2, i.e., when a bus buffer control signal 13 is set at logic level "0" with a signal 10 or 11 set at logic level "1" respectively, the input/output of the buffer 1 is set at a high impedance. Then the bus 5 is separated from the bus 6. Thus it is possible to protect the element 8 from noises and also to improve the capacity of the buffer 1.



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G 06 F 13/20　7165－5B

審査請求　未請求　発明の数 1　（全3頁）

⑤4発明の名称　ＣＰＵ周辺回路

⑳特　願　昭59－621
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⑦4代理人　弁理士　内原　晋

明　細　書

1. 発明の名称

ＯＰＵ周辺回路

2. 特許請求の範囲

ＯＰＵにそれぞれ接続されたアドレスバス，第一のデータバスと、前記アドレスバス，前記第一のデータバスを介して前記ＯＰＵにより制御されデータを記憶するメモリと、前記アドレスバスに接続され前記メモリを選択する手段と、前記第一のデータバスと第二のデータバスとに接続されるバスバッファと、前記第二のデータバスに接続される周辺素子と、前記メモリが選択され前記周辺素子がアクセスされないときは前記バスバッファが前記第一のデータバスと前記第二のデータバスとを分離し、前記周辺素子がアクセスされているときは前記バスバッファが前記第一のデータバスと前記第二のデータバスとを接続するように制御する手段とを有することを特徴とするＯＰＵ周辺回路。

3. 発明の詳細な説明

本発明はＯＰＵ周辺回路に関する。

〔従来技術〕

ＯＰＵとメモリが接続されるバスラインにおいて周辺素子でノイズが発生した場合、ＯＰＵとメモリ間での動作中であってもバスラインは周辺素子に対して開放されているので、周辺素子が数多く接続されていたり、周辺素子への配線が長く引き回されていたりして、バスラインのインピーダンスが高くなっている場合、バスラインにノイズが発生しやすくなり、その結果、メモリに間違ったデータが書きこまれたり、メモリから間違ったデータが読み出されるばかりでなく、間違った実行番地へプログラムの処理が進んでしまうという欠点があった。

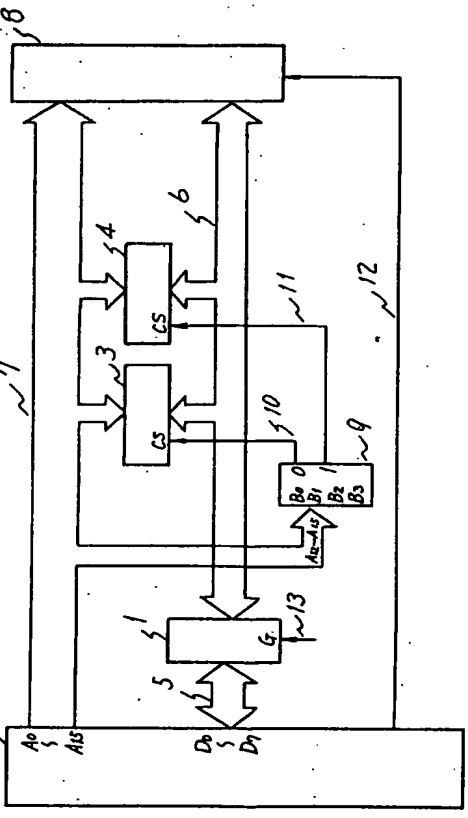
〔発明の目的〕

この発明の目的は上述のような従来の欠点を解消し、メモリ動作を保護できるＯＰＵ周辺回路を

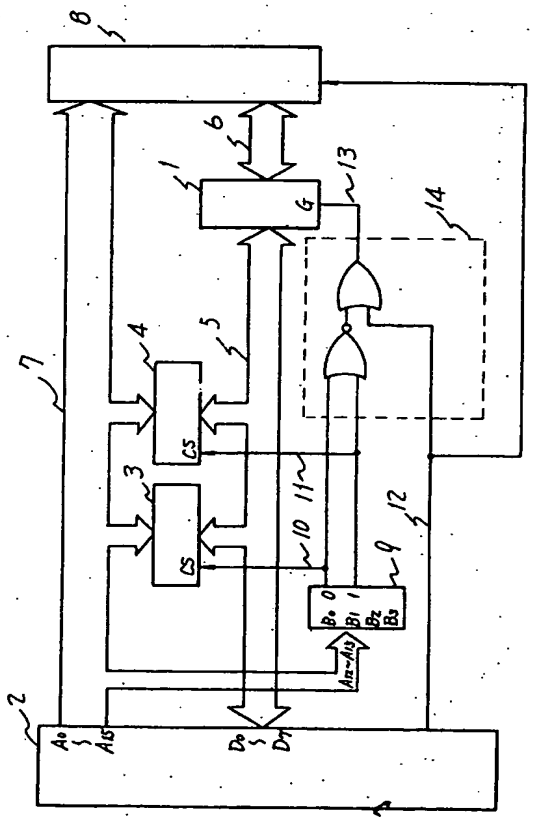
ス、8……周辺素子、9……[redacted]ナリーデシマルデコーダ、10……メモリセレクト信号、11……メモリセレクト信号、12……周辺素子アクセス信号、13……バスバッファ制御信号、14……バスバッファ制御回路。

代理人　弁理士　内原　晋

第1図



第2図



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CPU PERIPHERAL CIRCUIT

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[There are no amendments to this patent.]

Claim

CPU peripheral circuit characterized by the fact that it has: an address bus and a first data bus that are each connected to the CPU; a memory that stores data controlled by the aforementioned CPU via the aforementioned address bus and the aforementioned first data bus; a means that is connected to the aforementioned address bus and that selects the aforementioned memory; a bus buffer that is connected to the aforementioned first data bus and to a second data bus; a peripheral element that is connected to the aforementioned second data bus; and a means that performs control so that when the aforementioned memory is selected and the

aforementioned peripheral element is not accessed, the aforementioned bus buffer separates the aforementioned first data bus and the aforementioned second data bus, and when the aforementioned peripheral element is accessed, the aforementioned bus buffer connects the aforementioned first data bus to the aforementioned second data bus.

Detailed explanation of the invention

The present invention pertains to a CPU peripheral circuit.

Prior art

When noise is generated by a peripheral element on a bus line in which CPU and memory are connected, the bus line is released for the peripheral element even when there is an operation between the CPU and memory. Thus a large number of peripheral elements are connected, or the wiring to the peripheral elements is lengthened, which increases the impedance and generates impedance on the bus line. The result is that not only will erroneous data be written into the memory or erroneous data be read from the memory, but program processing may progress to erroneous execution addresses, which is a problem.

Objective of the invention

The objective of the present invention is to solve existing problems such as those above and to provide a CPU peripheral circuit that can protect memory operations.

Constitution of the invention

The CPU peripheral circuit of the present invention is characterized by the fact that it has: an address bus and a first data bus that are each connected to the CPU; a memory that stores data controlled by the aforementioned CPU via the aforementioned address bus and the aforementioned first data bus; a means that is connected to the aforementioned address bus and selects the aforementioned memory; a bus buffer that is connected to the aforementioned first data bus and a second data bus; a peripheral element that is connected to the aforementioned second data bus; and a means that performs control so that when the aforementioned memory is selected and the aforementioned peripheral element is not accessed, the aforementioned bus buffer separates the aforementioned first data bus and the aforementioned second data bus, and when the aforementioned peripheral element is accessed, the aforementioned bus buffer connects the aforementioned first data bus to the aforementioned second data bus.

Conventional example

The explanations below make references to the figures. Figure 1 shows a conventional example. Bus buffer (1) is connected to CPU (2) and data bus (5). Peripheral element (8), memory (RAM) (3), and memory (ROM) (4) are connected to common data bus (6). Bus buffer control signal (13) is fixed at logic level "1" and bus buffer (1) functions only as a two-way buffer. Selection of memory (RAM) (3) and memory (ROM) (4) is accomplished with memory select signals (10) and (11) from binary-decimal decoder (9). Here a case is shown where memory (RAM) (3) occupies addresses 0-FFFH and memory (ROM) (4) occupies addresses 1000H-1FFFH by decoding bits A_{12}-A_{13} of address bus (7).

Even when there is an operation between CPU (2) and memory (RAM) (3) or memory (ROM) (4) in Figure 1, data bus (6) is released to peripheral element (8). So noise generated in peripheral element access signal (12) by peripheral element (8) due to random factors may interfere with CPU (2) and memories (3) and (4) on data bus (6) and cause malfunctions.

Application example of the invention

Figure 2 is a block diagram that shows an application example of the present invention. CPU (2) and memory (3) and (4) are connected to data bus (5). Data bus (6) is connected to peripheral element (8) and is separated from bus (5) by bus buffer (1).

Next, the operation of bus buffer control circuit (14) will be explained. Memory select signals (10) and (11) will have a logic level "1" when their respective memory is selected, the peripheral element access signal will have a logic level "1" when the peripheral element is selected, and the bus buffer will be active when a logic level "1" is input to control input (G). When there is an operation between memory (3) or (4) and CPU (2), that is, only when memory select signal (10) or (11) is at a logic level "1" and peripheral element access signal (12) is at a logic level "0," bus buffer control signal (13) will be at a logic level "0." The input and output of bus buffer (1) will be high impedance, and data buses (5) and (6) are separated. In other cases, that is, when the peripheral element access signal is at a logic level "1," bus buffer (1) is always active, so no faults will occur in the operation between peripheral element (8), CPU (2) and memory (3) or (4).

Effect of the invention

In this way, with the present invention, memory operation can be protected from peripheral element noise and bus buffer performance can be improved. That is, no buffer is required between the CPU and memory, since the interface between NMOS devices is matched, and fan-out for the peripheral element will be increased by the amount corresponding to

removing the memory from the load relative to a conventional case where the memory acts as a load.

Brief description of the figures

Figure 1 is a block diagram that shows a conventional example. Figure 2 is a block diagram that shows one application example of the present invention.

(1) ... bus buffer, (2) ... CPU, (3) ... memory (RAM), (4) ... memory (ROM), (5) ... data bus, (6) ... data bus, (7) ... address bus, (8) ... peripheral element, (9) ... binary decimal decoder, (10) ... memory select signal, (11) ... memory select signal, (12) ... peripheral element access signal, (13) ... bus buffer control signal, (14) ... bus buffer control circuit.

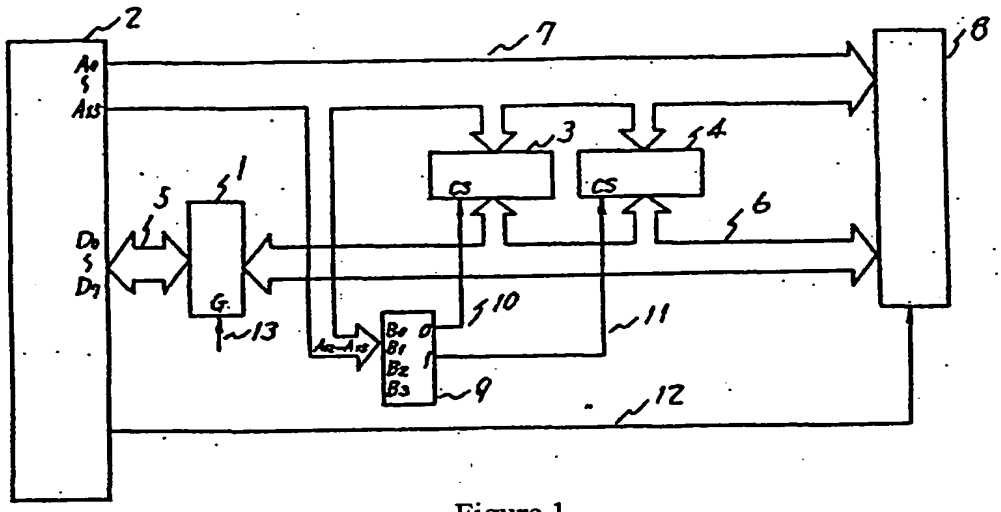

Figure 1

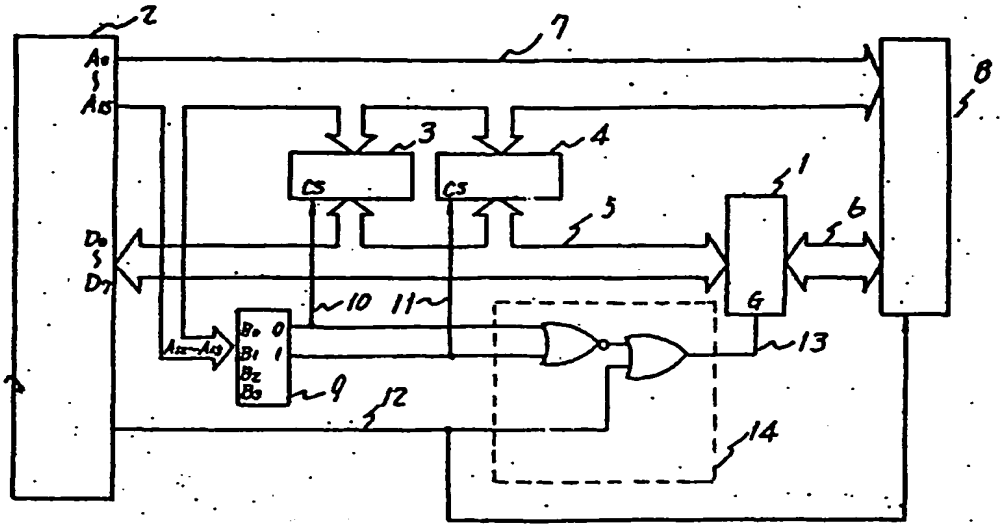

Figure 2